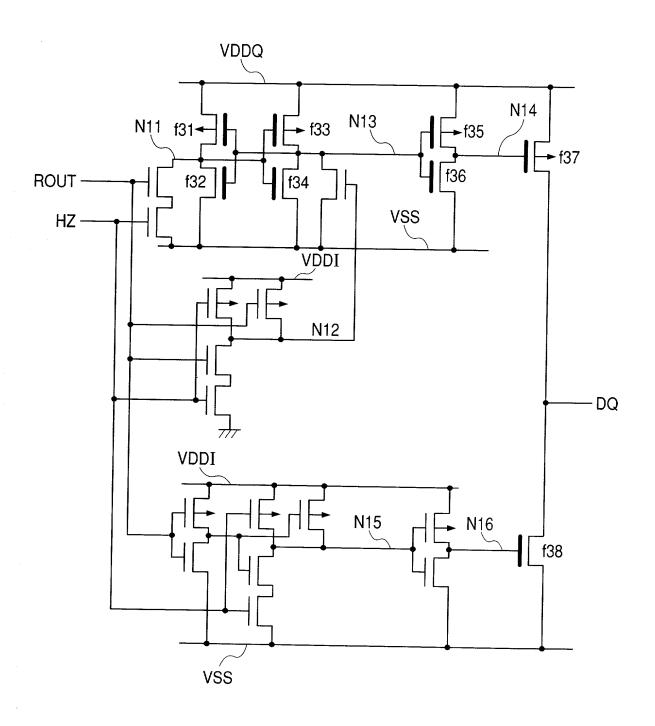
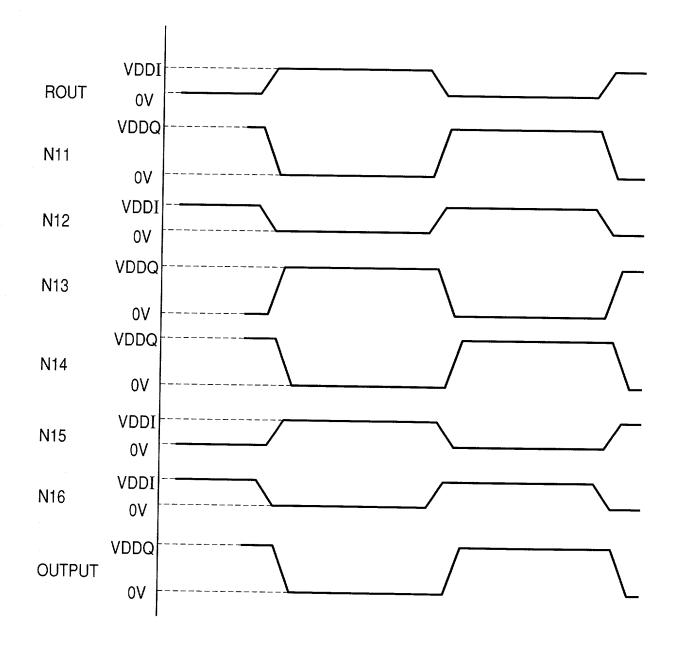


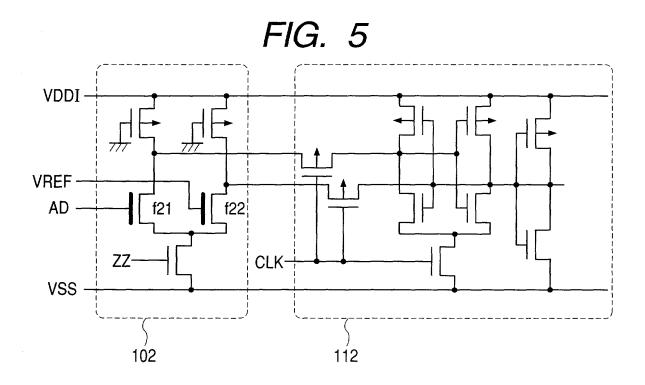
FIG. 3



1911 at 1821 at 1821 at 1821 at 1822 at 1823 at 1823 at 1824 a

FIG. 4





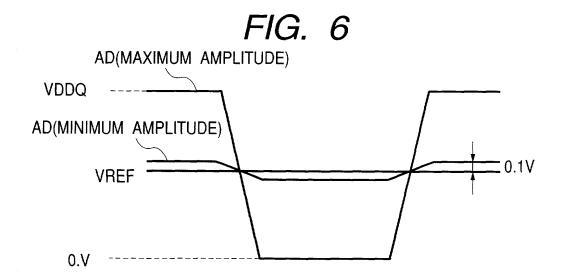
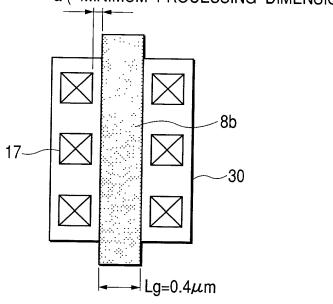


FIG. 7(a)

a (=MINIMUM PROCESSING DIMENSION)



3.3V WITHSTANDING MOS TRANSISTOR

FIG. 7(b)

a (=MINIMUM PROCESSING DIMENSION)

8c

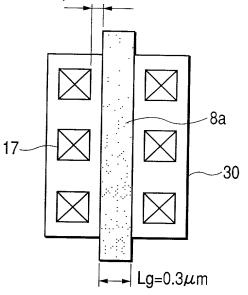
31

Lg=0.14µm

1.5V WITHSTANDING MOS TRANSISTOR

FIG. 8(a)

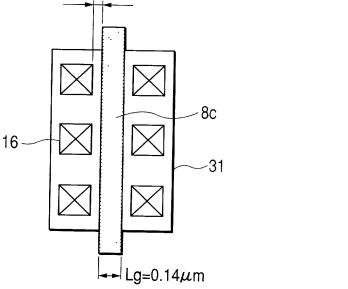
a (=MINIMUM PROCESSING DIMENSION)+ lpha



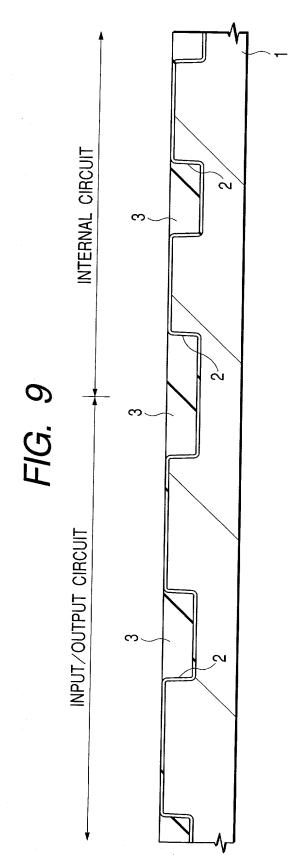
2.5V WITHSTANDING MOS TRANSISTOR

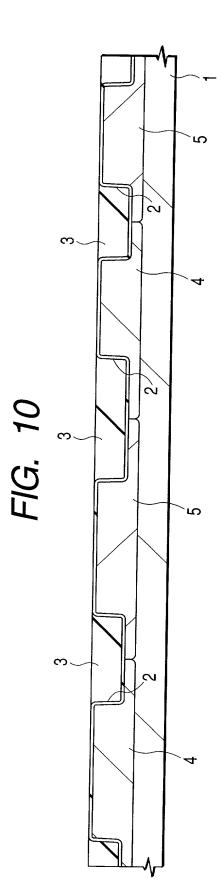
FIG. 8(b)

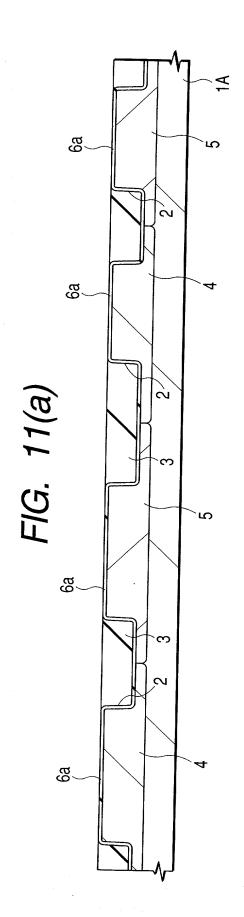
a (=MINIMUM PROCESSING DIMENSION)

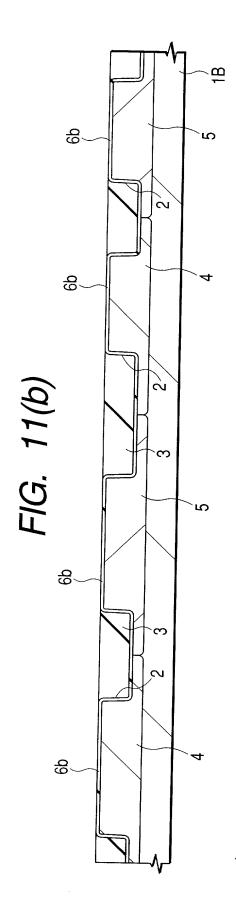


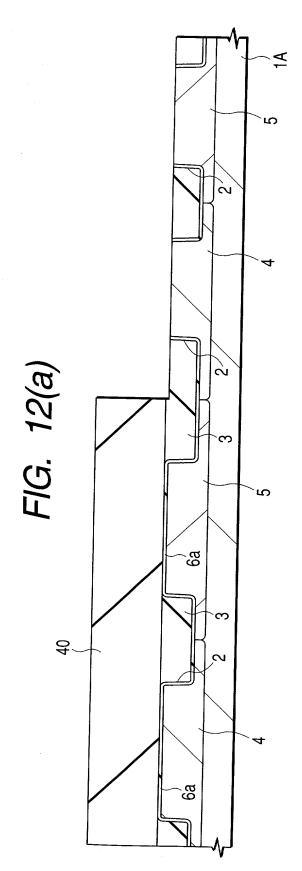
1.5V WITHSTANDING MOS TRANSISTOR

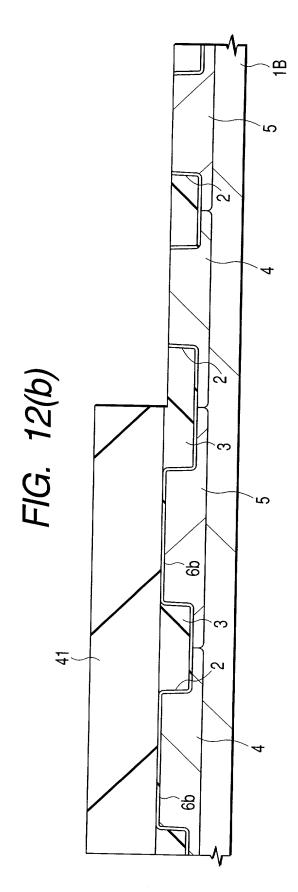


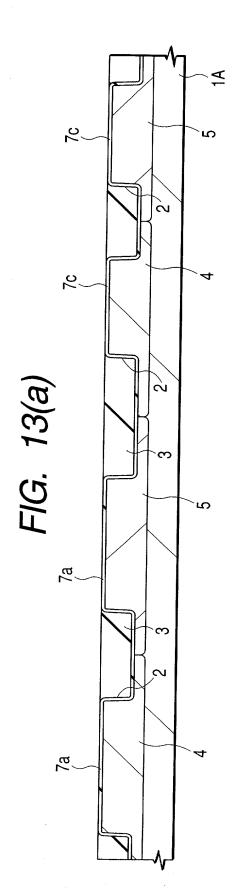


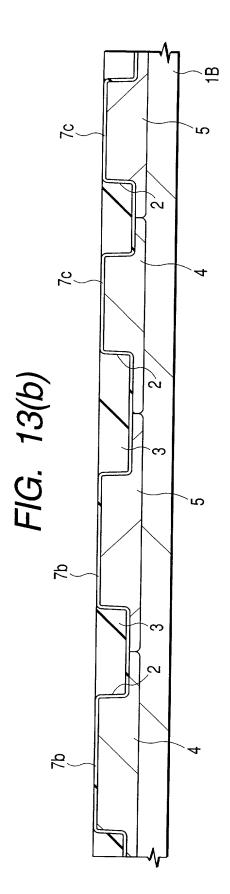


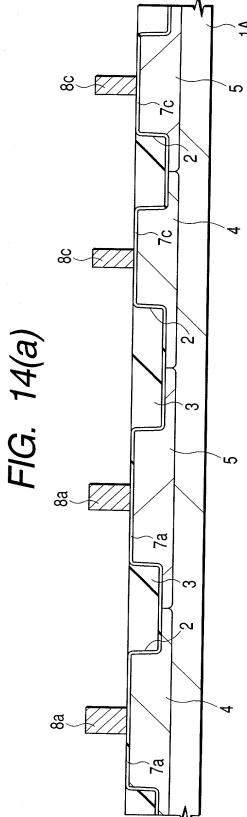


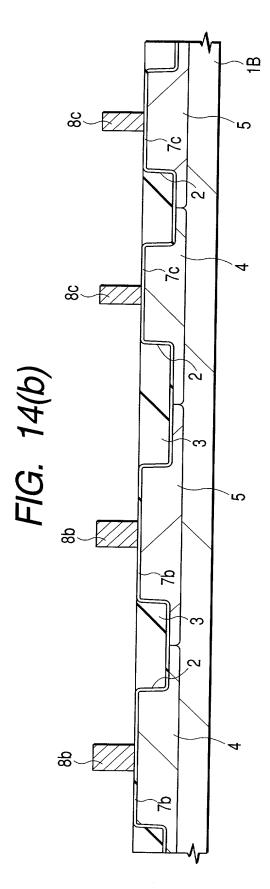




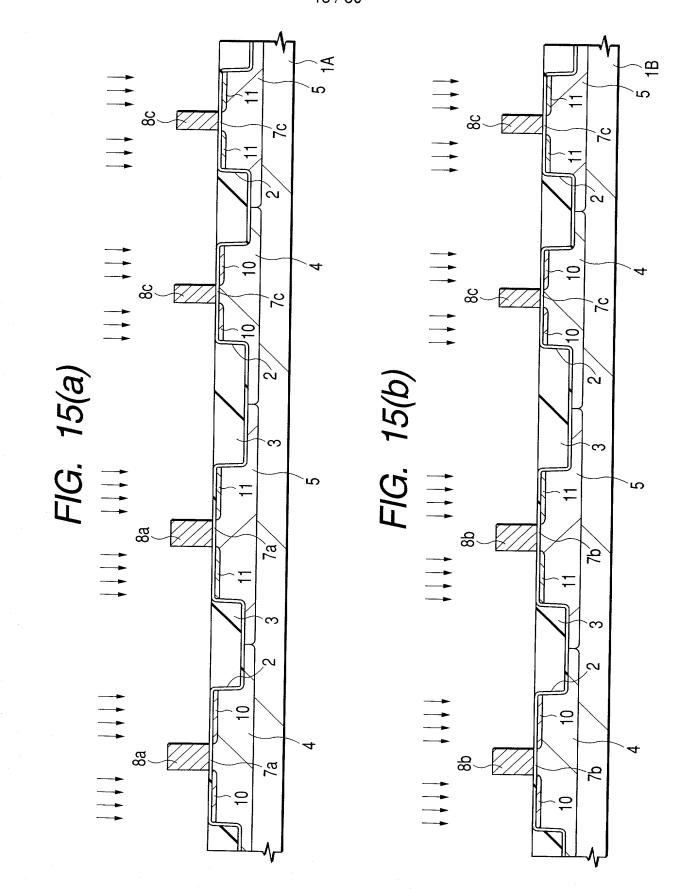


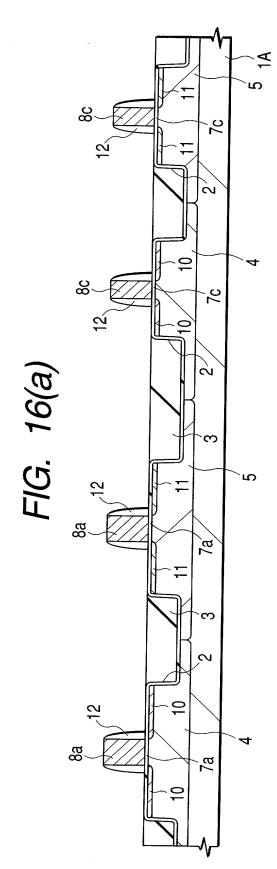


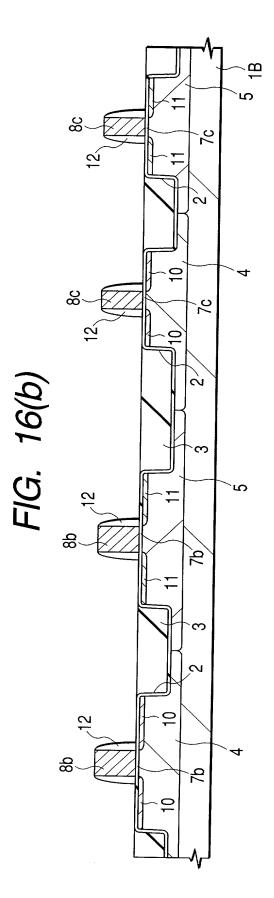


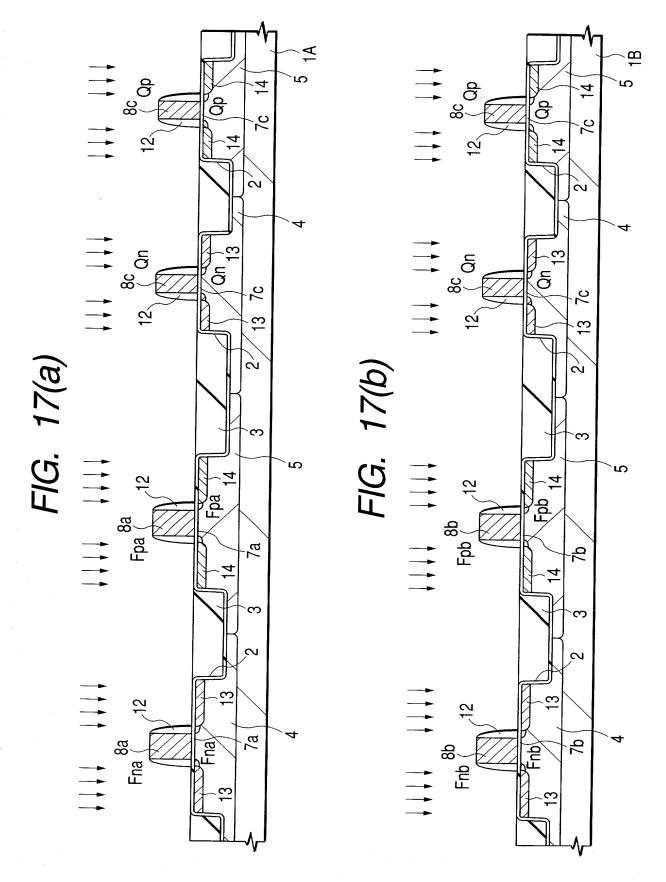


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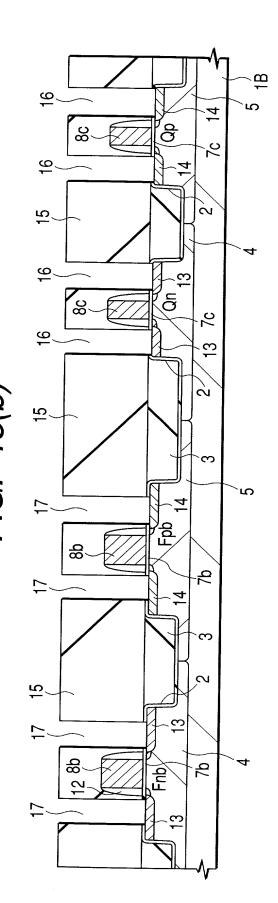








5 5, **7**a



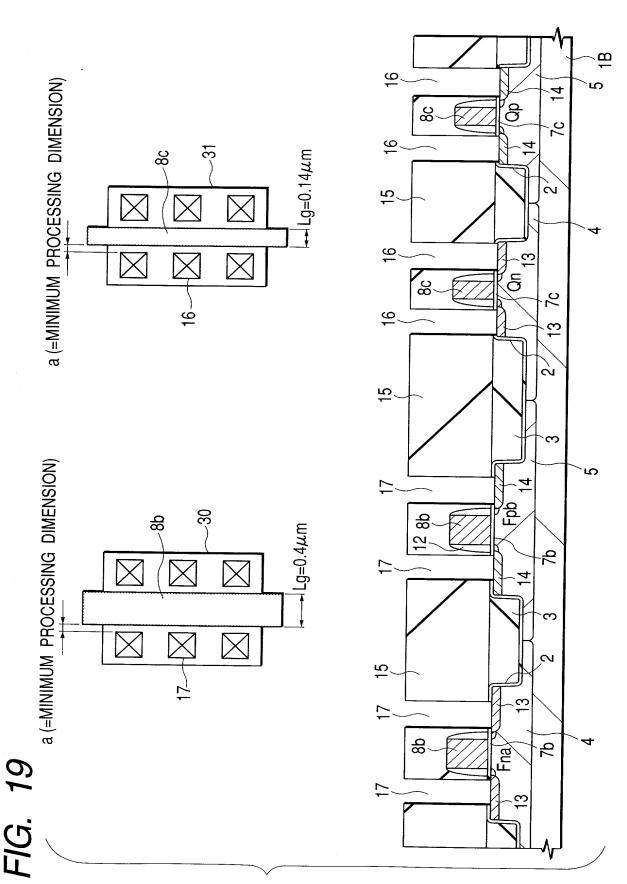
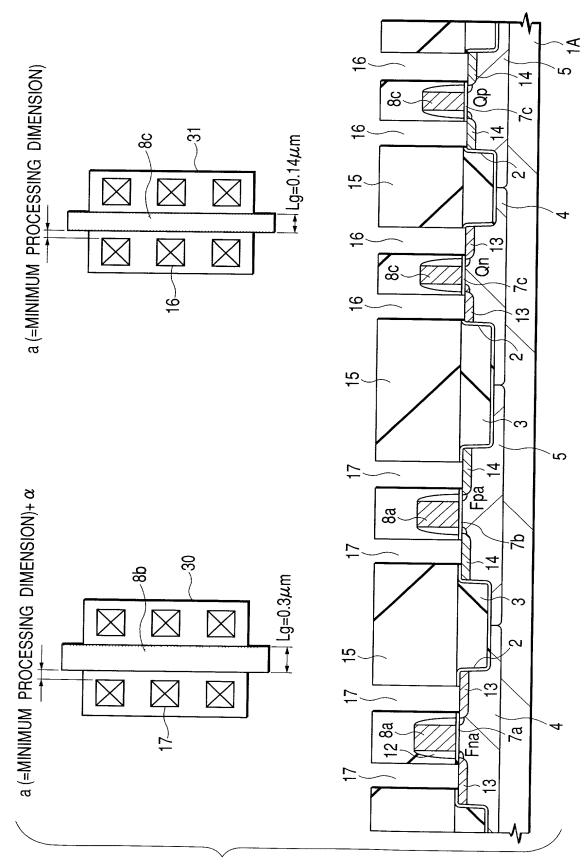


FIG. 20



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FIG. 21

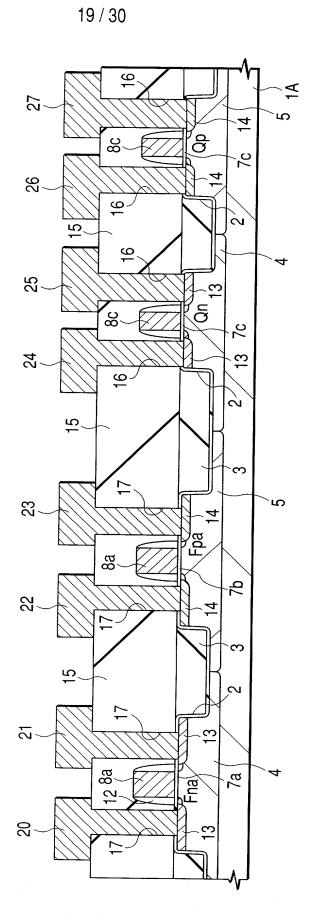
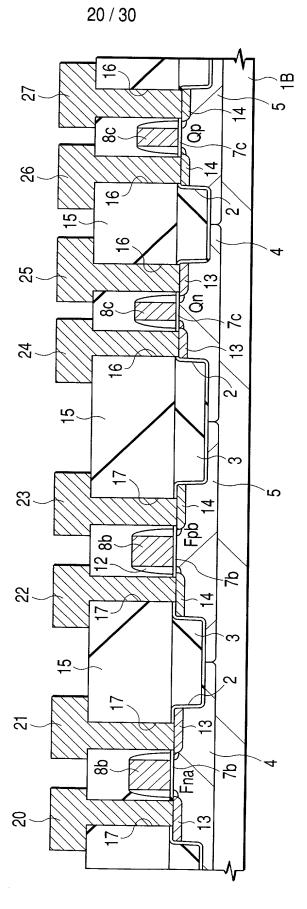
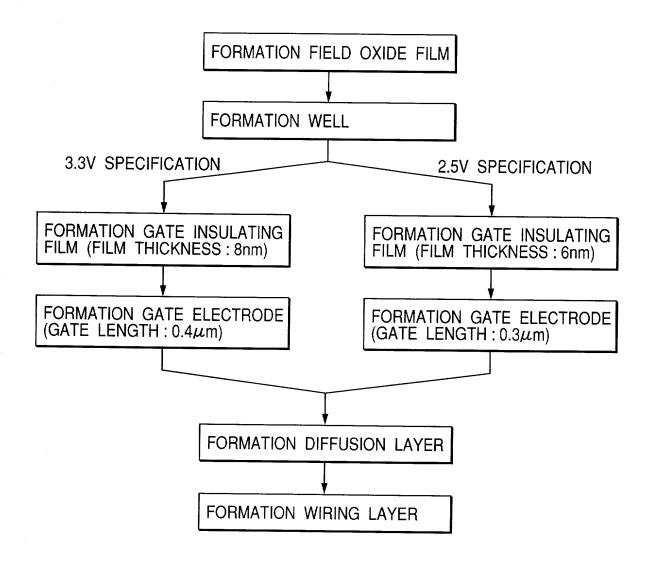


FIG. 22





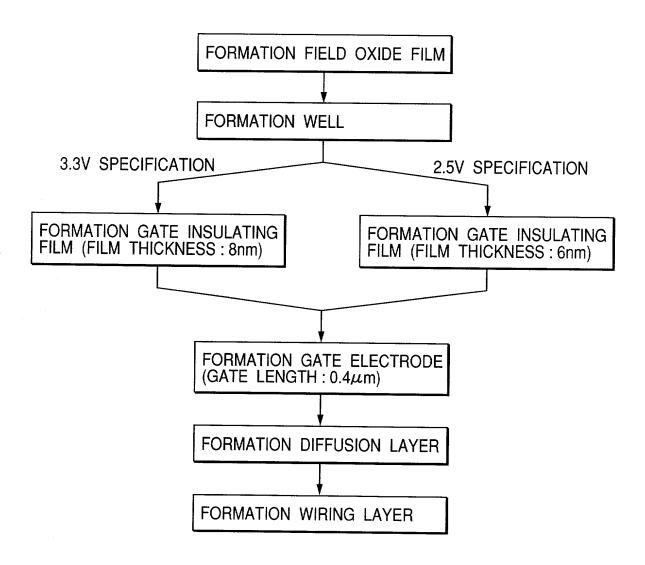
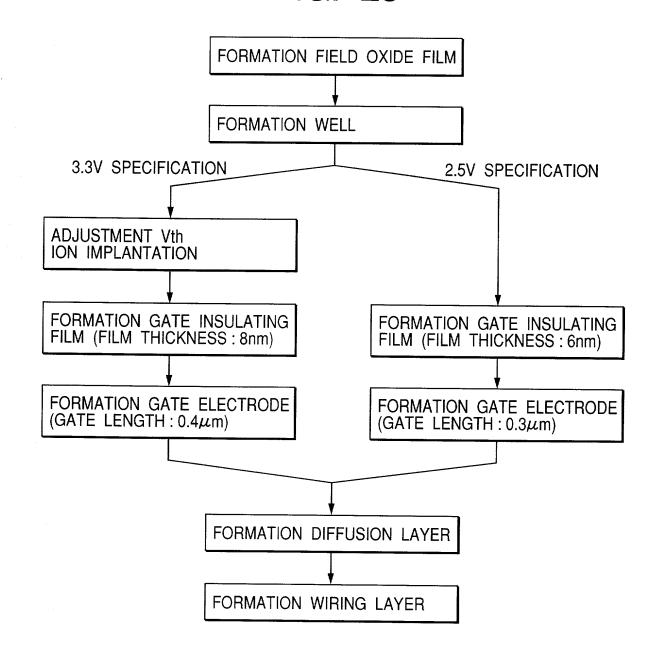
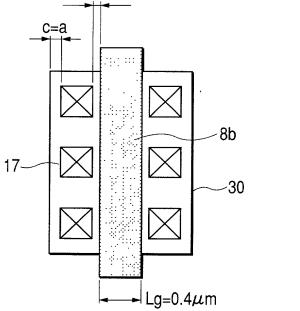


FIG. 25

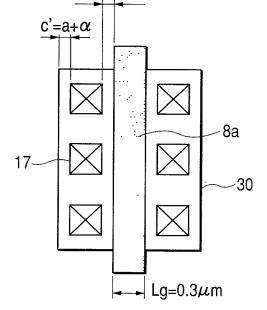


a (=MINIMUM PROCESSING DIMENSION)



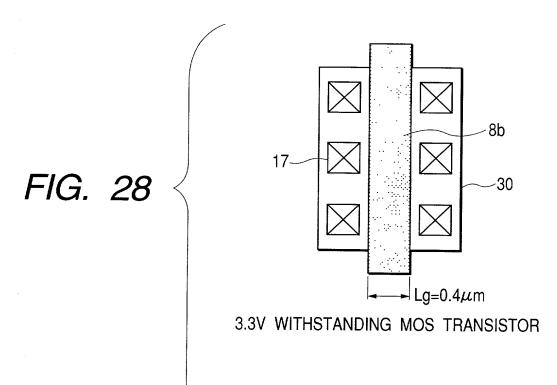
3.3V WITHSTANDING MOS TRANSISTOR

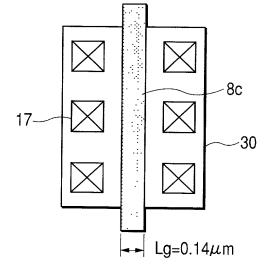
a (=MINIMUM PROCESSING DIMENSION)



2.5V WITHSTANDING MOS TRANSISTOR

SPECIFICATION	SUPPLY VOLTAGE	I/O SUPPLY VOLTAGE	INPUT SIGNAL LEVEL		SUPPLY VOLTAGE INTERNAL CIRCUIT
	VDD	VDDQ	VILmin	VIHmax	VDDI
3.3V SPECIFICATION	3.3V	3.3V	0V	VDDQ	1.5V
2.5V SPECIFICATION	2.5V	1.5V	0V	VDDQ	1.5V





2.5V WITHSTANDING MOS TRANSISTOR

SPECIFICATION	SUPPLY VOLTAGE VDD	I/O SUPPLY VOLTAGE VDDQ	INPUT SIG VILmin	NAL LEVEL VIHmax	SUPPLY VOLTAGE INTERNAL CIRCUIT VDDI
3.3V SPECIFICATION	3.3V	3.3V	0V	VDDQ	1.5V
2.5V SPECIFICATION	2.5V	2.5V	0V	VDDQ	1.5V

FIG. 30	GATE INSULATING FILM THICKNESS TOX	MINIMUM PROCESSING GATE LENGTH Lg	
3.3V WITHSTANDING MOS	8nm	0.4µm	
2.5V WITHSTANDING MOS	6nm	0.3µm	
1.5V WITHSTANDING MOS	3nm	0.14µm	

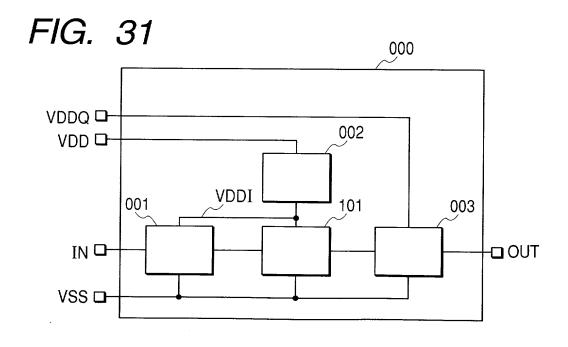


FIG. 32

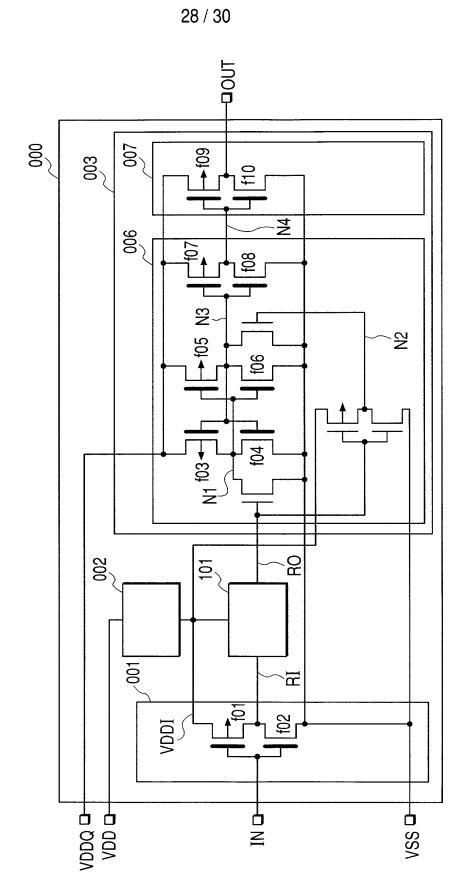


FIG. 33

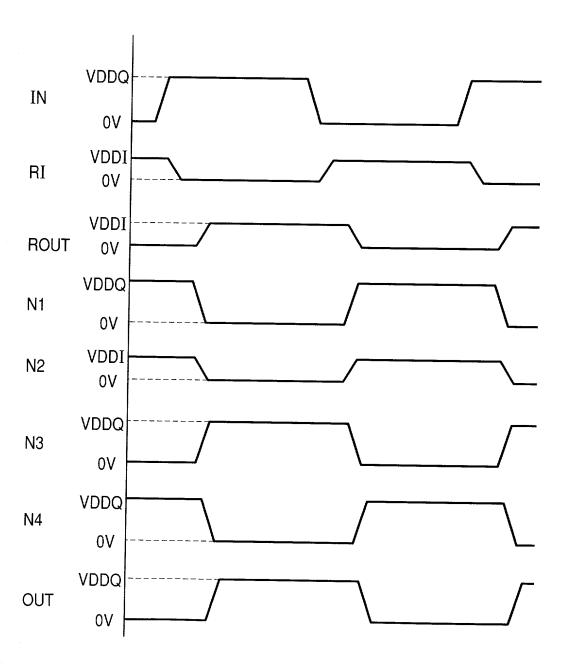


FIG. 34

